

# Comparison of Power Dissipation and Delay of Two Stage and Three stage Voltage Sense Amplifier

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**Abstract**— A three stage Voltage Sense Amplifier (VSA) with two inputs and single ended output is presented. A Sense Amplifier is responsible for detecting small input level differences at bit line voltages and amplifying it into a signal level that could be easily recognized as either high or low voltages. Cross coupled inverter is used for sensing the two differential inputs obtained from input stage. Results are obtained using CMOS technology in tanner environment. Latch-type voltage Sense Amplifier uses high impedance positive feedback mechanism. Delay and Power Dissipation are experimentally calculated. Total propagation delay of 26.08ns and power dissipation of 13.13 milliwatt is obtained in three stage Sense Amplifier.

**Index Terms**—Voltage Sense Amplifier, Cross Coupled Inverter, CMOS technology, Voltage Sensing, Latch-Type VSA.

## I. INTRODUCTION

SENSE Amplifiers are the basic circuits that are used in memory devices due to their ability for fast response and decisions. The Latch-Type Voltage Sense Amplifier circuits are used for obtaining the recognized voltage levels for the corresponding voltage levels on bit lines of memory devices. The conventional type voltage Sense Amplifier circuits provide high delays in decision making.

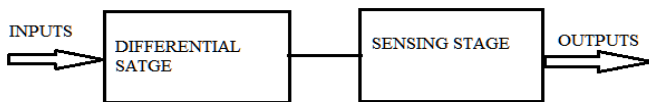


Fig.1. Block Diagram of Two stage Sense Amplifier

The above figure shows the block diagram of conventional Latch-type Voltage Sense Amplifier with double ended output. The first stage is the input differential Amplifier stage which provides the differential input to the sensing stage

. The sensing stage is a cross coupled inverter. The Sense

Amplifiers based on voltage sensing are widely used but this principle application of Sense Amplifiers becomes slow for low supply voltages and large memory designing. Various results are obtained at different values of the input DC level but accurate results are obtained at 0.7V.

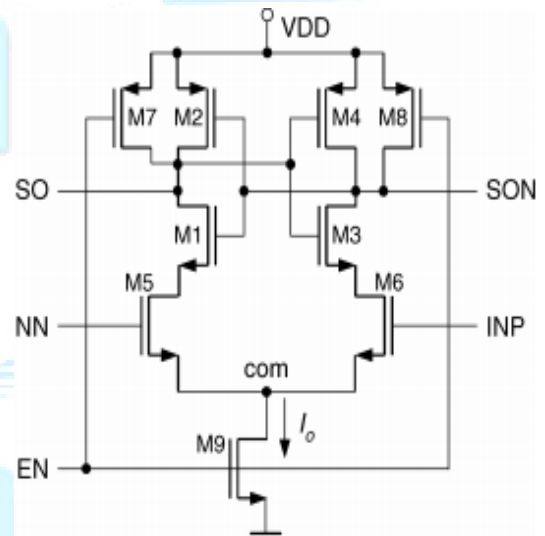


Fig.2 Latch-type voltage Sense Amplifier [1]

## II. PROPOSED THREE STAGE VOLTAGE SENSE AMPLIFIER

The conventional Voltage Sense Amplifier circuit contains two stages and two outputs are obtained. The three stage Sense Amplifier contains input stage, sensing stage and post Amplifier stage. The post Amplifier stage is used to give single ended output.

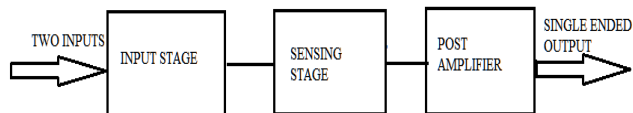


Fig.3. Block diagram of Three Stage Sense Amplifier

**A. INPUT STAGE:**

The input stage is a differential Amplifier circuit that provides differential output to sensing stage. The two inputs given to differential stage are INP and INN where INN is a constant DC level of 0.7V and INP piece-wise linear (PWL) voltage. Figure 4 shows the input differential stage of Sense Amplifier where to inputs INN and INP are taken.

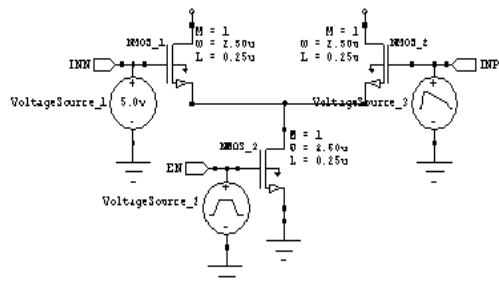


Fig.4. Differential Input Stage

**B. SENSING STAGE:**

Second stage is sensing stage which comprises of cross coupled inverter and two outputs SO and SON are obtained. The outputs are obtained on the transition of the enable signal. Figure.5. shows the sensing stage of Sense Amplifier.

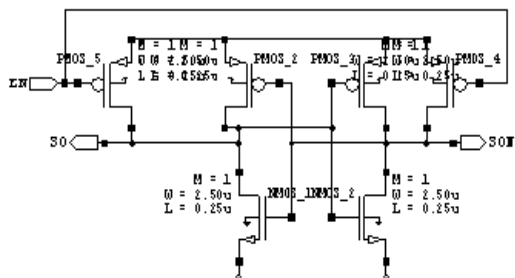


Fig.5. Cross coupled inverter in sensing stage giving two outputs.

**C. POST AMPLIFIER STAGE:**

The sensing stage provide double ended output therefore the third stage is employed so as to convert the output in single ended, this is done using post Amplifier. Fig shows the post

Amplifier used as third stage in Sense Amplifier.

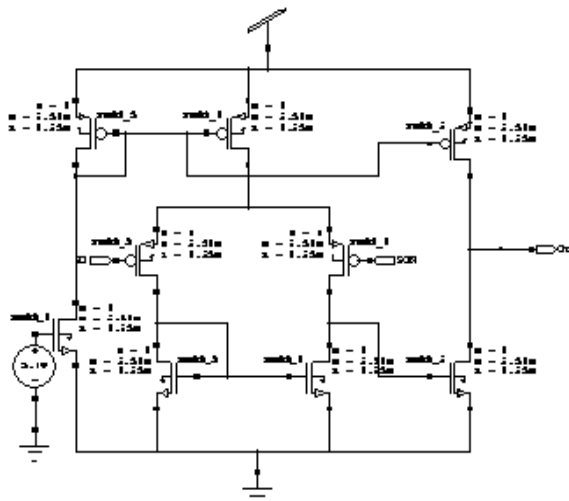


Fig.6. Post Amplifier as third stage for giving a single ended output

**III. TRANSIENT BEHAVIOUR**

The transient behavior is shown in fig.7. The current is not drawn in off stage and only leakage current is associated with the MOSFETs. The signals INN and INP are inputs to the transistors NMOS\_1 and NMOS\_2. Transistors NMOS\_1 and NMOS\_2 are differential Amplifier that give the differential input to the cross coupled inverter formed by transistors PMOS\_3, PMOS\_2, NMOS\_1 and NMOS\_1. The output terminals SO and SON are pulled to V<sub>DD</sub> by transistors PMOS\_5 and PMOS\_4. The enable signal starts the sensing operation by turning on transistor NMOS\_2. When EN signal is high then circuit is pulled up and when EN is low circuit is pulled down. When EN is high and the inputs are applied on transistors NMOS\_1 and NMOS\_2 we assume that SON is in high state then transistor PMOS\_2 is turned off and we get a low output corresponding to SO. The current flow stops when EN is low.

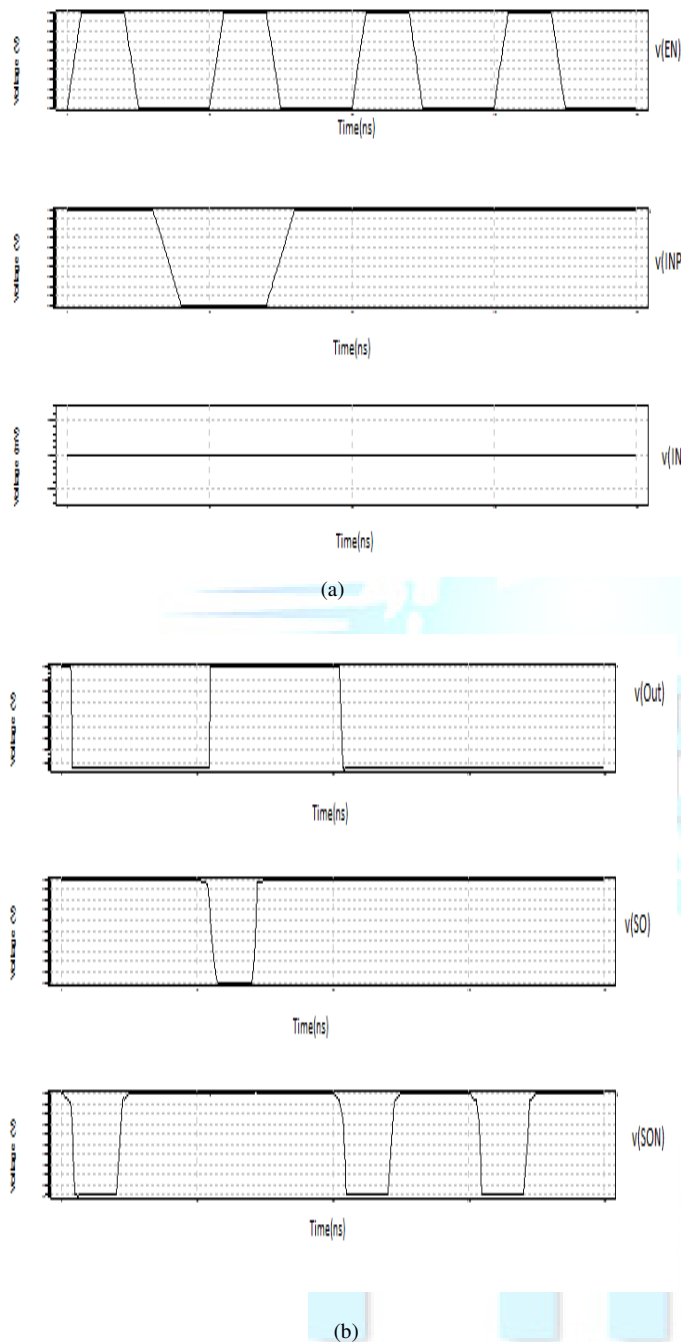


Fig.7 Transient behavior of Latch-type Sense Amplifier(a) Input signal INN and INP and enable signal.(b) V(out),Output of third stage and outputs SON and SO, outputs of second stage

The two outputs of stage two are applied to third stage NMOS\_1 and NMOS\_2 which are driven by the two load transistors PMOS\_5 and PMOS\_1 whose output drives PMOS\_2 which generates the overall output voltage V(out).

#### IV. RESULTS

The results of two Stage Sense Amplifier and three Stage Sense Amplifier are compared. The comparison has been done using Tanner Environment. Delay of circuit is improved and

circuit response faster to the input voltage swing.

Table:1

SENSE AMPLIFIER	DELAY (ns)	POWER DISSIPATION (Watts)
TWO-STAGE	26.08	9.855e-005
THREE STAGE	18.05	1.313e-002

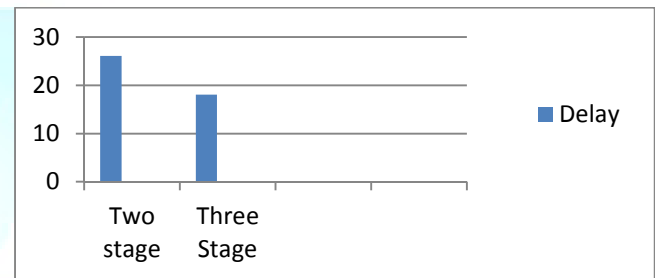


Fig.8. Bar- Chart of delay (ns) of Two Stage and Three Stage Sense Amplifier

#### V. CONCLUSION

Three stage voltage Sense Amplifier has faster response and has less power dissipation. The two stage voltage Amplifier has been compared with three stage Sense Amplifier circuit and a graph of comparison of delay has been plotted between two stage results and three stage results giving a better performance of three stage Voltage Sense Amplifier.

#### ACKNOWLEDGEMENT

The authors wish to thank College Management for providing the environment required for completing this research work. Authors are thankful to Chairman, Dean, Head of Department, Lecturers and Colleagues for their support. Special thanks to National Institute of Electronics And Information Technology, Gorakhpur for providing us the laboratory environment.

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